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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,586	08/22/2003	Katsunori Ueno	FUJI:141A	9944

7590 04/09/2004

Marc A. Rossi
ROSSI & ASSOCIATES
P.O. Box 826
Ashburn, VA 20146-0826

EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/646,586	UENO, KATSUNORI	
	Examiner	Art Unit	
	Samuel A Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 25 March 2004.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 5-11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 5-11 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of group II, claims 5-11 drawn to a method of forming semiconductor device is acknowledged.

Drawings

2. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect can be deferred until the application is allowed by the examiner.

3. Figures 10-12 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Specification

4. The disclosure is objected to because of the following informalities:

page 13, line 20, refers to "fig. 4(a) through 4(e)". There is no figure 4(e) in the drawing. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5-6 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Palmour US patent No. 5,629,531.

Regarding claims 5, 6 and 11, Palmour teaches (figs. 3A and 3B) a method for manufacturing a silicon carbide n channel MOS semiconductor device, comprising the steps of preparing a silicon carbide substrate (11) comprising a p base region (12), an n+ source region (14) and an n+ drain region (15); forming a gate insulating film (19) on a surface of the p base region; forming a gate electrode (18) on the gate insulating film; and forming first (16) and second (17) main electrodes on the silicon carbide substrate such that current is allowed to flow between the first and second main electrodes, wherein the surface layer of the p base region (12) is formed by epitaxial growth (epi-layer, see fig. 3A).

The limitation that current flowing between the first and second main electrodes is controlled by controlling an electron concentration of an inversion layer that is induced in a surface layer of the p base region located under the gate insulating film when a positive voltage is applied to the gate electrode, is the basic functional characteristics of a MOSFET device.

Palmour does not teach the limitation of an effective acceptor concentration in the vicinity of an interface between the p base region and the gate insulating film to be in a range of 1×10^{13} to 1×10^{16} cm^{-3}. Palmour neither explicitly teaches that the p base region is formed by ion implantation.

Parameters such as doping concentration and doping energy in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Furthermore Palmour teaches that ion implantation is commonly used to implant epitaxial layers of silicon carbide (col. 5, lines 60-67)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the acceptor concentration as claimed in order to improve current conduction.

It would also have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the ion implantation process in the process of Palmour in order to form an n-channel MOS transistor.

The limitations that the acceleration voltage and dose amount are controlled so that the acceptor concentration in the vicinity of the interface between the p base region and the gate insulating film is made lower than that in an inner part of the p base region or wherein ions of donor impurities are implanted into the surface layer of the p base region in an amount that does not form an n-type region that is not depleted with zero bias, so that the effective acceptor concentration in the vicinity of the interface between the p base region and the gate insulating film is made lower than that in an inner part of the p base region are not given patentable weight, because a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

7. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Palmour in view of Suzuki et al. US patent No. 5,329,141.

Regarding claim 7, Palmour teaches substantially the entire claimed process of claim 6 above except explicitly stating that the ions of donor impurities are implanted into the surface layer of the p base region in a dose amount "x" that is in a range represented by: $1 \times 10^{11}\ cm^{-2} < x < 5Q_B/q$.

It is conventional and also taught by Suzuki doping a p-type region with a donor impurity in the formation of a light-emitting device (see abstract).

Furthermore parameters such as doping concentration and doping energy in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to dope the p layer of Palmour's process as taught by Suzuki in order to increase recombination current. It would also have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the doping concentration in the range as claimed in the process of Palmour in order to increase the recombination current.

Regarding claim 8, Palmour teaches substantially the entire claimed process of claim 6 above including the donor impurities comprise nitrogen (col. 2, lines 38-50).

8. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Palmour, Suzuki and in view of Shenoy et al. (High voltage planar 6H-SiC Accufet, Materials science forum Vols. 264-268 (1998) pp 993-996).

Regarding claims 9 and 10, Palmour teaches substantially the entire claimed process of claim 6 above except explicitly stating that conducting heat treatment for activating impurities introduced by ion implantation wherein the heat treatment is carried out at a temperature of 1000 to 1500°C.

It is conventional and also taught by Shenoy activating impurities by annealing impurity regions in the temperature range as claimed in the process of forming a transistor device (pages 994, device fabrication section).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the process of annealing at the specified temperature in the process of Palmour as taught by Shenoy in order to make a transistor that is functional.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References B and C are cited as being related to silicon carbide structures.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

SAG
April 2, 2004